Errata

Title & Document Type: Word Generator 8016A, Operating & Service Manual

Manual Part Number: 08016-90004

Revision Date: 1990

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual provides the best information we could find. It may be incomplete or contain dated information, and the scan quality may not be ideal. If we find a better copy in the future, we will add it to the Agilent website.

Support for Your Product

Agilent no longer sells or supports this product. You will find any other available product information on the Agilent Test & Measurement website:

www.tm.agilent.com

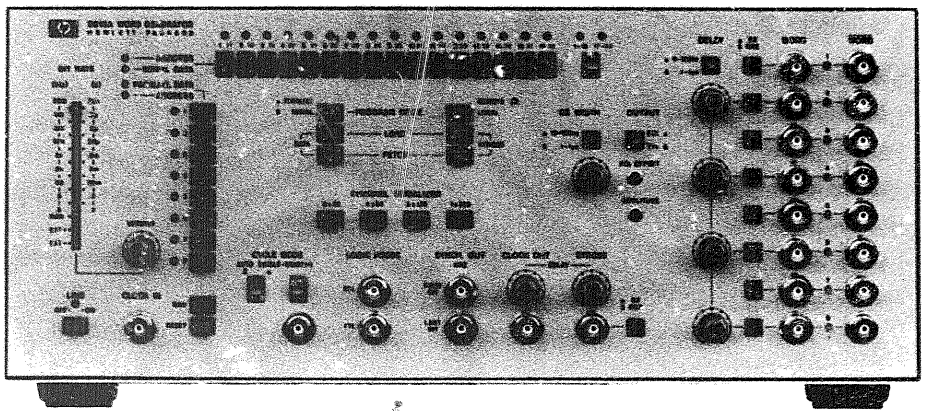
Search for the model number of this product, and the resulting product page will guide you to any available information. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available.

Agilent Technologies

Operating and Service Manual
Word Generator 8016A
Publication Number 08016-90004
Published on January 1, 1990

OPERATING AND SERVICE MANUAL

8016A
WORD GENERATOR



HEWLETT hp PACKARD

SECTION 1

INTRODUCTION

1–1 The model 8016A is a multichannel word generator incorporating the following features:

- 50 MHz clock;
- 9 x 32 bit memory maximised by use of a channel serializer;
- 6 independent delay circuits;
- output levels and transition times complying to ECL and TTL test specifications;
- RZ or NRZ format with variable RZ width;
- free programmability of bit pattern;
- finally, a particularly useful feature, the PARALLEL/SERIAL switch to eliminate laborious conversion work by the user before entering date.

1–2 In contrast to the wide-ranging features, the front panel is designed with simplicity the objective. The number of data-setting pushbuttons is optimised to a single column/single row arrangement. Each pushbutton controls a one-bit buffer register and is neatly complemented by an LED which indicates the status of the register i.e. illuminated for data "1". Data can be loaded in parallel or serial form dependent on the selected position of the PARALLEL/SERIAL switch. When data is loaded into the buffer registers, a single switch transfers the data to the 288-bit high speed memory. If data in any memory address needs to be checked or transferred, there is a fetch facility for returning the required data to the buffer registers, where it is indicated by LEDs.

1–3 The output of data can also be in parallel or serial form. In parallel, data is output as 32 words each 8 bits wide; in serial, data is output as 8 words each 32 bits long. When in the serial mode, the output channels can be serialized via a channel serializer to produce word lengths of up to 256 bits. The channel serializer also determines the function of the strobe output. The strobe can function either as a ninth data channel (channel serializer in the 8 x 32 position only) or as a 32-bit trigger word which can be assigned to any or all words in the serialized 8-word data frame. Additional outputs for synchronizing purposes are provided in the form of first and last bit outputs and the clock output.

1–4 Applications

1–5 The 8016A is designed for flexibility as demonstrated by the free programmability of bit pattern, which combined with the short cycle time (50 MHz clock), makes the 8016A especially effective for determining worst case conditions in I.C. testing e.g. high speed testing of critical areas of memory. The free programmability of bit pattern is also useful both for component evaluation, by enabling small quantities of devices to be tested by unskilled personnel, and for feeding controlled bit patterns into data bus lines e.g. data communications systems, time-sharing systems, telemetry systems etc.

1–6 Optional Versions

1–7 8016A – Option 001: This enables the bit pattern to be programmed from a calculator, a computer, or any other controller which is compatible with the HP Interface Bus (HP-IB).

1–8 8016A – Option 002: Provides a card reader, which can program the bit pattern of the 8016A Opt. 001 in approximately 2 seconds.

Table 1–1. Specifications

DATA CAPACITY

Number of channels: 8 data channels plus 1 strobe channel.

Number of bits per channel: 32 (fixed)

Total bit capacity: 288

Data can be loaded in parallel or serial form depending on the position of the PROGRAM MODE switch. The data is loaded via a single row and single column of push-buttons, each pushbutton controlling a one-bit buffer register.

SERIAL CAPACITY

One word consists of 32 bits in serial. A front panel switch serializes words to form a frame.

Serial formats:

9 words on 9 channels, including strobe word, each 32 bits long.

4 frames on 4 channels, each consisting of 2 words or 64 bits.

2 frames on 2 channels, each consisting of 4 words or 128 bits.

1 frame on 1 channel consisting of 8 words or 256 bits.

PARALLEL CAPACITY

Parallel Format:

32 words each 9 bits wide (including strobe bits)
64 words each 4 bits wide
128 words each 2 bits wide

DATA OUTPUTS

Two separate outputs per channel, one for normal and one for complement.

Amplitude: TTL or ECL voltage levels, selectable by front panel control.

Source impedance: 50Ω

Delay: four channels can be separately delayed between 0ns and 1 μsec with reference to the channels 1, 3, 5 or 7.

Two ranges: 0ns 100ns
0.1μs 1μs

Ranges are common to all delayable channels. Channels have individual vernier controls.

Delay jitter: 0.1% + 50ps.

Skewtime: Skewtime of undelayable channels (3, 5, 7) with reference to channel one: ± 1ns.

FORMAT

RZ or NRZ, separately selectable for each data channel and strobe channel.

RZ width: 10nsec to 1μsec in two ranges. Vernier provides continuous adjustment within ranges. Range switch and vernier is common to all channels.

Width jitter: ± 0.2% + 50ps.

AUXILIARY OUTPUTS

First bit: Corresponds with parallel word one or with the first bit of serial word. Format is NRZ.

Last bit: Corresponds with the last parallel word or with the last bit of the last word of a frame. Format is NRZ.

Clock: Delivers one trigger pulse per bit. Format is RZ.

Clock pulse width: controlled by RZ-width control.

Clock pulse may be delayed between 0ns and 1μs with reference to channels 1, 3, 5 or 7.

Table 1–1. (cont'd)

STROBE WORD

In addition to the LOAD DATA and FETCH DATA pushbuttons, there are LOAD STROBE and FETCH STROBE pushbuttons. The strobe word length is 32 bits but can be extended by repetition to 256 bits.

The strobe word may be delayed between 0ns and 1μsec with reference to channels 1, 3, 5 or 7.

Amplitude of Aux. Outputs: TTL or ECL voltage levels selectable by front panel control.

Source impedance: 50 ohms.

PROBE POWER

ECL: −5.2V dc ± 10%; 80mA

TTL: +5V dc ± 10%; 100mA

BIT RATE

Internal, 0.5 Hz to 50 MHz in eight ranges. Vernier provides continuous adjustment within ranges.

External: dc up to 50 MHz or manual triggering.

CLOCK INPUT

Repetition rate: 0 to 50 MHz

Trigger pulse width: ⩾ 10nsec

Trigger amplitude: selectable by internal switches on Bit Rate board A5. Max. Amplitude: ± 7V at 100% duty cycle.

Ext. +: setting of bit rate control (for TTL)

Amplitude: ⩾ +2.0V

Input impedance: ⩾ 1KΩ to GND.

Ext. +:

Amplitude: ⩾ +1.0V

Input impedance: 50Ω to GND

Ext. −: setting of bit rate control (for ECL).

Amplitude: ⩽ −1.6V

Input impedance: 50Ω to −2V

Ext. −: Trigger level adjustable at Potentiometer A5R114 from +1V to −1V.

Input impedance: 50Ω to GND.

RECYCLING

Auto Mode: data is recycled continuously.

Single Cycle (2 modes):

a) One word generated for each cycle command.

b) Words generated as long as the cycle command is active. Last word always completed. If channels are serialized, the serialized word (64 bits, 128 bits, 256 bits) is always completed.

Period between cycle commands: Byte (frame) length plus 200ns

External Command Specifications

Amplitude: > +2V, < +10V

Width: > 12ns

Input impedance: 1KΩ

MANUAL RESET

Auto cycle: All channel outputs are set to "0". The next clock pulse after RESET generates parallel word one.

Single cycle: All channel outputs are reset to word pause. A rear panel switch sets the pause level to zero or to the level of the last bit.

Table 1–1. (cont'd)

PULSE CHARACTERISTICS

The level of all output signals is controlled by a TTL–ECL switch. Adjusts for amplitude and offset. Source impedance is 50Ω.

TTL (across 50Ω): HIGH LEVEL variable from 2.5V to 1V. LOW LEVEL ⩽ +0.2V.

Transition times: < 3.0ns (First/Last Bit Trigger < 4.0ns).

ECL (across 50Ω): HIGH LEVEL OFFSET variable from –0.9V to +1.1V. Amplitude variable from ⩽ 0.4V to ⩾ 1.0V.

Transition times: ⩽ 2.5ns (First/Last Bit Trigger < 4.0ns).

REMOTE PROGRAMMING OPTION (001)

Provides an interface card to the Hewlett-Packard Interface Bus (HP-IB).

The bit pattern can be programmed via any controller which is HP-IB compatible.

CARD READER OPTION (002)

Provides an optional card reader that programs the bit pattern in the 8016 via HP-IB and the interface card. The interface card has to be ordered separately as option 001.

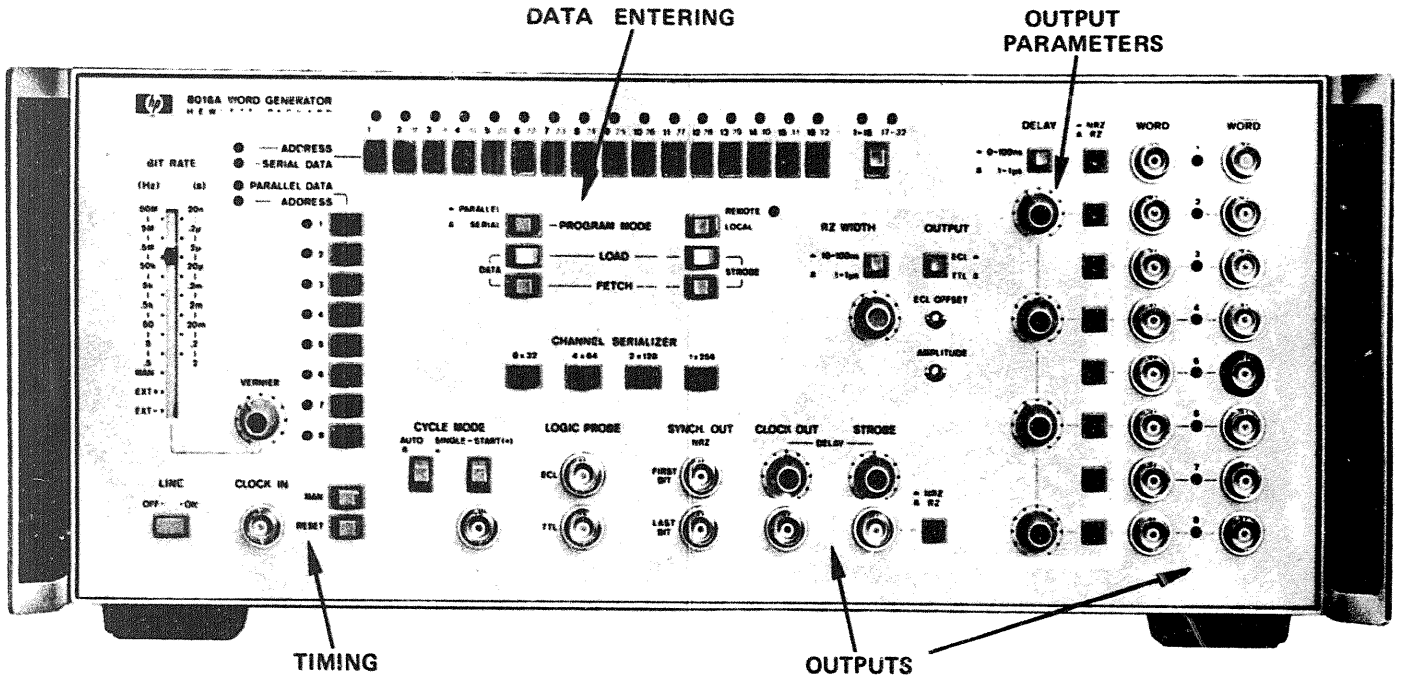
GENERAL

Operating temperature range: 0°C to 50°C

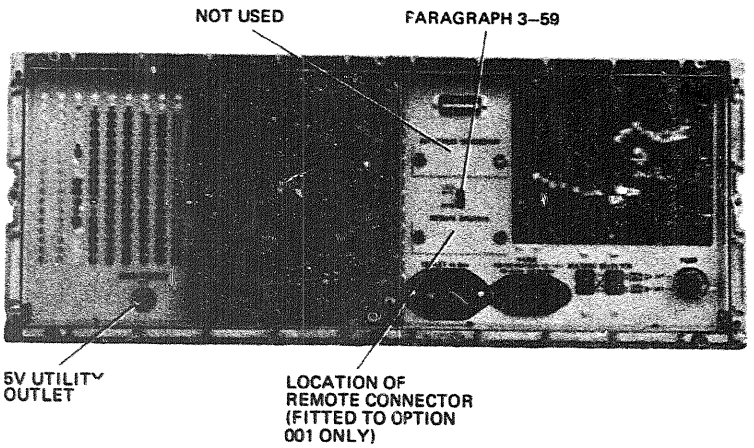
Power requirements: 100/120/220 or 240V +5%, –10%, 48 Hz to 66 Hz, 200 VA (maximum).

Weight: net 14,5 kg (31,96 lbs); shipping 16 kg (35,27 lbs).

Dimensions: 460 x 475 x 178 mm (18 x 18,650 x 7 ins.).



Front Panel — Functional Areas



Rear Panel — Controls and connectors

Figure 3–1. Controls and Connectors

3–1 GENERAL

3–2 The following instructions apply to model 8016A, 8016A – Option 001 and 8016A – Option 002. Ignore instructions which do not apply to your instrument.

3–3 CONTROL FUNCTIONS

3–4 The 8016A front panel can be divided into 4 main control functions:

- Data Entering
- Outputs
- Output Parameters
- Timing

3–5 Figure 3–1 clearly illustrates each functional area. The controls/indicators within each area are fully described in the following text.

3–6 DATA ENTERING

3–7 Figure 3–2 shows the relevant front panel area for data entering. (The REMOTE/LOCAL switch is only relevant to option 001 described in appendix A.)

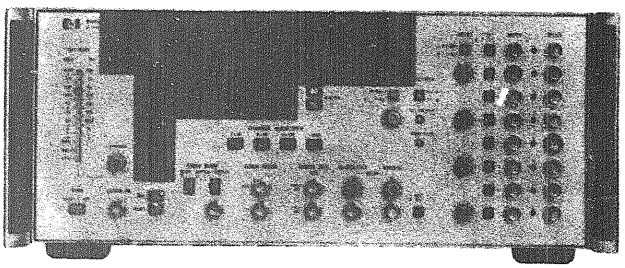
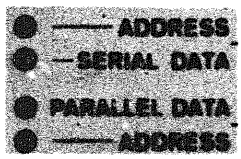


Figure 3–2. 8016A – Data Entering

3–8 Data can be loaded in parallel or serial form selectable via the PARALLEL/SERIAL pushbutton switch. If PARALLEL is selected, then the pushbutton column is used for data-setting, and the pushbutton row for memory addressing. If SERIAL is selected, then the functions of the pushbutton row and column are reversed i.e. row for data-setting, column for memory addressing. A group of 4 LEDs located to the left of the pushbutton column/row arrangement provide a visual indication of the functions, the top 2 LEDs relating to the row function, the bottom 2 LEDs relating to the column function e.g.



The illuminated first and third LEDS provide a visual indication that the pushbutton row is being used for addressing memory, and the pushbutton column for data-setting.

3–9 Each pushbutton controls a one-bit buffer register, and the status of each register is indicated by an LED located alongside (column) or above (row) the corresponding pushbutton i.e. illuminated for a logic "1".

3–10 Parallel Loading

3–11 Data can be loaded one word (8 bits parallel) at a time into one or more of 32 word locations in the memory. The pushbutton column is utilized for data-setting and the pushbutton row for memory addressing. Each pushbutton in the row can address two memory word locations, dependent on the selection of the 17th pushbutton which assigns the 16 pushbuttons to the appropriate half of the row i.e. "1–16" or "17–32". LEDs provide a visual indication of the range selected.

3–12 When the address(es) is selected and the data is set into the buffer registers, the LOAD DATA pushbuttomust be operated to transfer the data from the buffer registers to the selected memory location(s).

3–13 If data in any memory location needs to be checked or transferred, there is a 'fetch' facility which provides a non-destructive read-out from the memory to the display register. To operate this facility, first select the required memory address (via the pushbutton row), then depress the FETCH DATA pushbutton. The data in the selected word address will be indicated by the LED

column adjacent to the pushbutton column. If more than one word address is selected prior to operating the FETCH DATA pushbutton, only the word with the highest address number is displayed, e.g. word addresses, 1, 3 and 5 selected, only one word address 5 is displayed. To transfer data, select the new word address and operate the LOAD DATA pushbutton.

3–14 Serial Loading

3–15 Data can be loaded 16 bits at a time into one or more of 8 word locations in the memory, each word location corresponding to a channel. The pushbutton column is utilized for memory addressing and the pushbutton row for data-setting. Each pushbutton in the row can set two bits in the 32-bit word dependent to the selection of the 17th pushbutton i.e. "1–16" or "17–32".

3–16 When the address(es) is selected and the data is set into the buffer registers, the LOAD DATA pushbutton must be operated to transfer the data from the buffer registers to the selected memory location(s).

3–17 As in 'parallel loading", if data in any word location needs to be checked or transferred, the 'fetch' facility provides a non-destructive read-out from the memory to the display register. To operate the fetch facility, select the required memory address (via the pushbutton column) and the required half of the word (via the 17th pushbutton), then depress the FETCH DATA pushbutton. The data in the selected word address will be indicated by the LED row location above the pushbutton row. If more than one address is selected prior to operating the FETCH DATA pushbutton, the contents of the selected word addresses are gated (OR'ed) to produce the LED display.

3–18 Loading 00, 01, 10, 11 Pattern

3–19 This facility provides a useful means for fast memory loading e.g. 256 bit checker-board pattern set by operating 29 pushbuttons only.

3–20 The method is best described by taking a single pattern i.e. "0" as an example. Hold the last two buffer registers (15–31 and 16–32 to "00" and simultaneously depress the FETCH DATA pushbuttons. On release, all buffer registers in the row will be set to "0". Operate the DATA LOAD pushbutton to transfer the pattern to memory.

3–21 Similarly for patterns "01", "10" or "11", except that the last two buffer registers are held to the required pattern.

3–22 OUTPUTS

3–23 Figure 3-3 shows the front panel area which is relevant to the following description of the outputs.

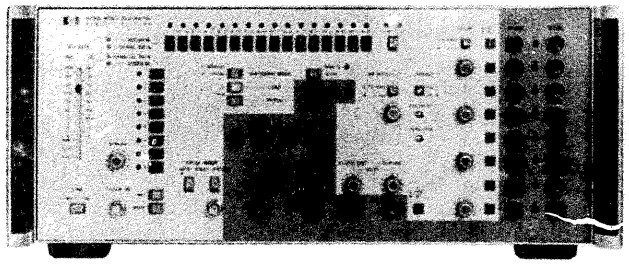


Figure 3–3. 8016A – Outputs

3–24 The outputs of the 8016A can be divided into two main categories:

– Data Outputs
– Auxiliary Outputs

3–25 Data Outputs

3–26 Normally, there are 8 data output channels, each channel providing normal and complement 32-bit signals. When the CHANNEL SERIALIZER is in the 8 x 32 position, the strobe output is a ninth data output channel.

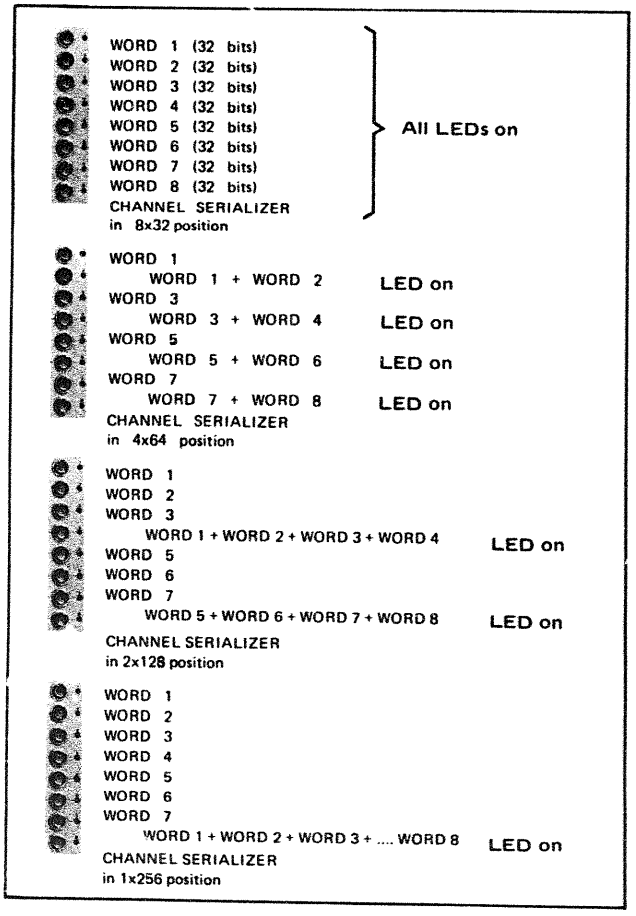


Figure 3–4. Channel Serializer

3–27 **Data Serialization.** The 8 output channels can be serialized (multiplexed) to give four channels each outputting a 64-bit word, two channels each outputting a 128-bit word or one channel outputting a 256-bit word. The channels outputting the serialized data are indicated by an illuminated LED, whilst the other channels continue to output a 32-bit word repetitively.

3–28 When the CHANNEL SERIALIZER is in operation, both the normal signals and the complement signals are serialized.

3–29 Auxiliary Outputs

3–30 The auxiliary outputs include the synch. outputs (first, last bit), clock output, strobe output and the probe power outputs.

3–31 **Synch Outputs.** There are two synch. outputs, one corresponding to the first bit of the data word, and the other corresponding to the last bit of the serial data frame, the data frame being 32 bits, 64 bits, 128 bits or 256 bits long depending on the CHANNEL SERIALIZER selection. Both outputs are in NRZ format (seeparagraph 3–38 for description of NRZ format).

3–32 **Clock Output.** This provides an output pulse at the rate set by the BIT RATE controls. The format is RZ.

3–33 **Strobe Output.** The strobe channel has 2 functions depending on the position of the channel serializer. It can function either as a ninth data channel, or as a 32-bit trigger word which can be assigned via the pushbutton column to the words with the serialized data frame. Figure 3–5 relates the position of the channel serializer to the data words available for assigning the strobe word.

3–34 Independent of both the strobe function and the PARALLEL/SERIAL switch setting, the strobe word is programmed via the pushbutton row, and transferred to memory by operation of the LOAD STROBE pushbutton. In addition, a FETCH STROBE facility, which is operated by simply pressing the FETCH STROBE pushbutton, shows both the strobe content (LED row) and the strobe assignment (LED column).

3–35 **Probe Power.** A unique feature of the 8016A is the LOGIC PROBE facility. This facility provides power sources for the HP 10525 E (ECL) logic probe, the HP 10525 T (TTL) logic probe, the HP 10526 T logic pulser or any other comparable instrument.

CHANNEL SERIALIZER SELECTION	OPERATIONAL 'COLUMN' PUSHBUTTONS	COMMENT
8 x 32	NONE	The strobe cannot be assigned to any 'data word' but functions as a ninth data channel. Data is set via the pushbutton row and transferred to memory via the LOAD STROBE pushbutton.
4 x 64		The strobe word can be assigned to one or both of data words 1 and 2 in the serialized data frame. Pushbuttons 3 – 8 have no control over strobe assignment.
2 x 128		The strobe word can be assigned to any or all of words 1 – 4 within the serialized data frame. Pushbuttons 4 – 8 have no control over strobe assignment.
1 x 256		The strobe word can be assigned to any or all of words 1 – 8 within the serialized data frame.
N.B.	Word 1 is the normal 32-bit output from Channel 1, Word 2 the normal 32-bit output from Channel 2, etc.	

Figure 3–5. Channel Serializer/Strobe Assignment

3–36 OUTPUT PARAMETERS

3–37 Figure 3–6 shows the front panel area which is relevant to the following description of the output parameters.

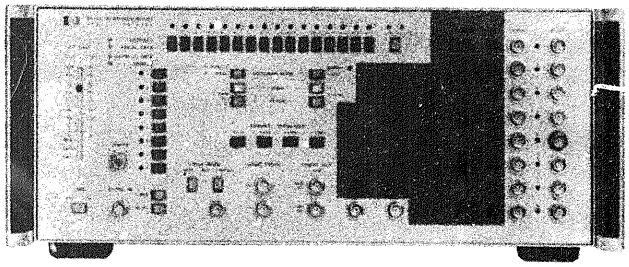


Figure 3–6. 8016A – Output Parameters

3–38 RZ/NRZ Formats

3–39 Each data channel and the strobe channel is provided with an independent RZ/NRZ format pushbutton switch. When a switch is set to "RZ", a logic "1" output from the associated channel returns to zero before the bit period ends. If the switch is set to "NRZ" then the associated output signal does not return to zero unless the following bit is zero. The significance of "return to zero" and "non-return to zero" is shown in Figure 3–7.

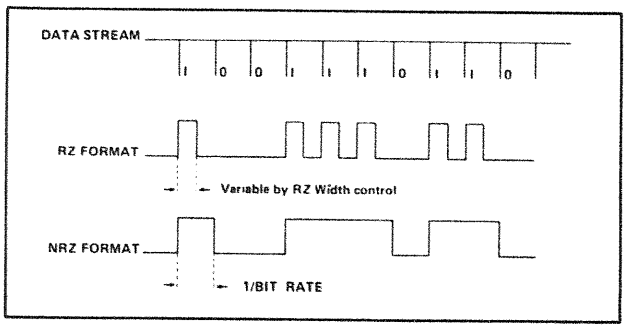


Figure 3–7. Comparison of RZ and NRZ Formats

3–40 RZ Width

3–41 An additional control is provided for varying the RZ width. All output channels in RZ format and the clock output are changed simultaneously by this one RZ width control. The width can be varied up to a maximum of 50% of the bit period. At high frequencies, this maximum is reduced to 40% of the bit period. (A bit period scale is provided adjacent to the BIT RATE slider).

3–42 A pushbutton located above the RZ WIDTH control enables one of two RZ width ranges to be selected i.e. 10ns – 100ns or .1μs – 1μs.

3–43 Delay

3–44 Data channels 2, 4, 6, 8, the strobe channel and the clock output can be delayed independently with respect to the fixed data channels 1, 3, 5 and 7, **within a common range.**

3–45 Two delay ranges are provided, 0 – 100ns, or .1μs – 1μs selectable via a single pushbutton switch.

3–46 The delay is also limited by the bit rate period. The maximum delay is 40% of the bit period. In the higher frequency range, the maximum delay is reduced to 10% of the bit period.

3–47 TTL or ECL Levels

3–48 All outputs (data, strobe, clock and synch) are simultaneously at TTL levels or ECL levels, selectable via a single pushbutton switch.

3–49 A screw vernier is also provided to vary the amplitude of the output signals (again simultaneously), irrespective of whether TTL or ECL is selected.

3–50 For ECL, an additional screw vernier (common to all outputs) is provided for adjusting the ECL offset independently of the amplitude.

3–51 These controls can be combined to produce:

- pulse levels as specified for most TTL (0V/3V)
- worst case levels for TTL (0.8V/2.0V)
- pulse levels for ECL powered form 0V/ –5.2V
- pulse levels for ECL powered from +2V/ –3.2V.

3–52 Figure 3–8 illustrates TTL and ECL signals and their associated parameters.

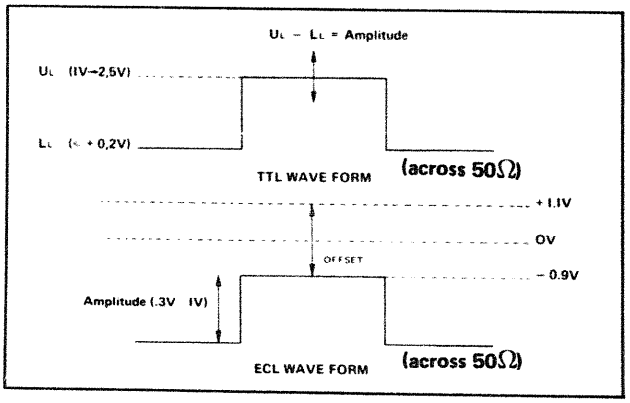


Figure 3–8. ECL and TTL Waveforms.

3–53 TIMING

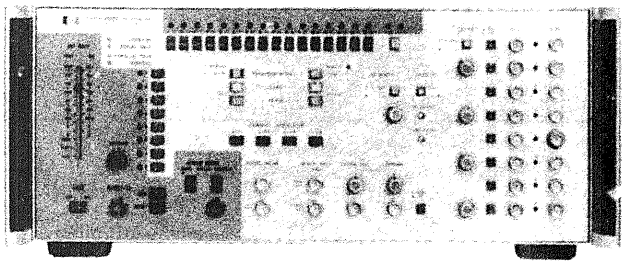


Figure 3–9. 8016A – Timing

3–54 Figure 3–9 shows the relevant front panel area for the following description of the timing controls.

3–55 Single/Auto Cycle

3–56 A pushbutton switch selects the auto mode or single cycle mode.

3–57 In the auto mode, data is recycled continuously.

3–58 In the single cycle mode, each cycle command from the START pushbutton (or an electrical trigger at the cycle command input) generates one cycle per channel, the length of this cycle depending on the selected position of the CHANNEL SERIALIZER. e.g. with the CHANNEL SERIALIZER in the 2 x 128 position, a 32-bit word is output from channels 1, 2, 3, 5, 6, 7, and a 128-bit word is output from channels 4 and 8. If the cycle command is from an external source, one cycle or multiple cycles per channel are generated, dependent on the selected position of switch A6S1 (Figure 3–12). One cycle is generated if position "1" is selected; multiple cycles are generated if position "2" is

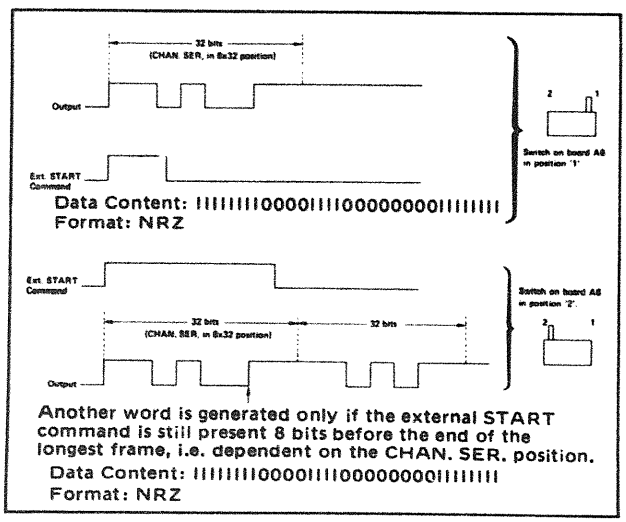


Figure 3–10. External Command/Single Cycle Mode

selected. The last cycle is always completed even if the cycle command ends during the cycle.

3–59 Also in the single cycle mode, a slide switch at the rear of the 8016A selects the output level during the pause between cycles. The level can either remain at the level of the last bit output (unless the format is RZ, in which case the last bit is output one more), or it will return to "0", as illustrated in Figure 3–11.

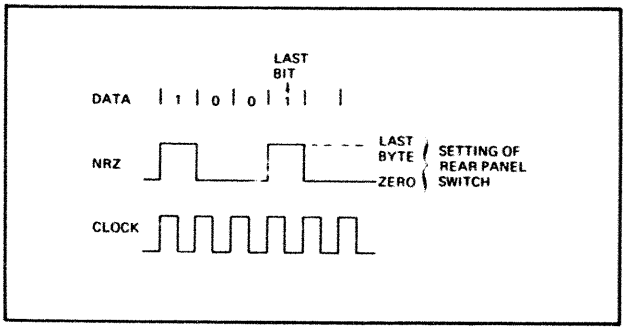


Figure 3–11. Pause level in RZ

3–60 Internal Clock

3–61 The internal clock is set via the BIT RATE and VERNIER controls and runs at 50 MHz down to 0.5 Hz, being digitally divided down in decades.

3–62 The BIT RATE control is provided with two scales i.e. a bit rate scale and a corresponding bit period scale.

3–63 External Clock

3–64 There are two BIT RATE control settings for an external clock, external positive (EXT +) and external negative (EXT –).

3–65 The EXT + setting allows the clock to be provided from TTL levels. An internal switch (A5S1, Figure 3–12) changes the input resistance from 50Ω – GND to 1kΩ – GND. The factory setting of this switch is 50Ω – GND, but by putting this switch to the 1kΩ – GND position, the external clock can be fed directly from TTL gates.

3–36 The EXT – setting is mainly for ECL levels. An internal switch (A5S2) changes the input resistance from 50Ω → –2V to 50Ω → GND. For the 50Ω → GND setting, which is the factory setting, the threshold level may also be varied between ± 1V via a potentiometer (A5 R114) located alongside the switch. By varying the threshold level, the external clock can be provided by any ECL level.

3–67 Manual Clock

3–68 When the BIT RATE control is set to MAN, a bit is output from each channel every time the MANUAL button is pressed.

3–69 In the Auto Cycle Mode, the RESET pushbutton puts all outputs to zero thus ensuring that the first operation of the MANUAL pushbutton outputs the first bit. In the Single Cycle Mode, the RESET pushbutton puts all outputs to the pause level defined by the switch at the rear of the 8016A (see para 3–42).

N.B. The MANUAL and RESET pushbuttons are only operational when the BIT RATE slider is set to the MAN position.

3–70 A feature of the manual clocking mode is that the LEDs associated with the row/column arrangement of data-setting pushbuttons indicate both the address (row LEDs), and the data content (column LEDs), of the output byte. This feature, together with the logic probe, can be used for truth-table testing of combinatorial networks.

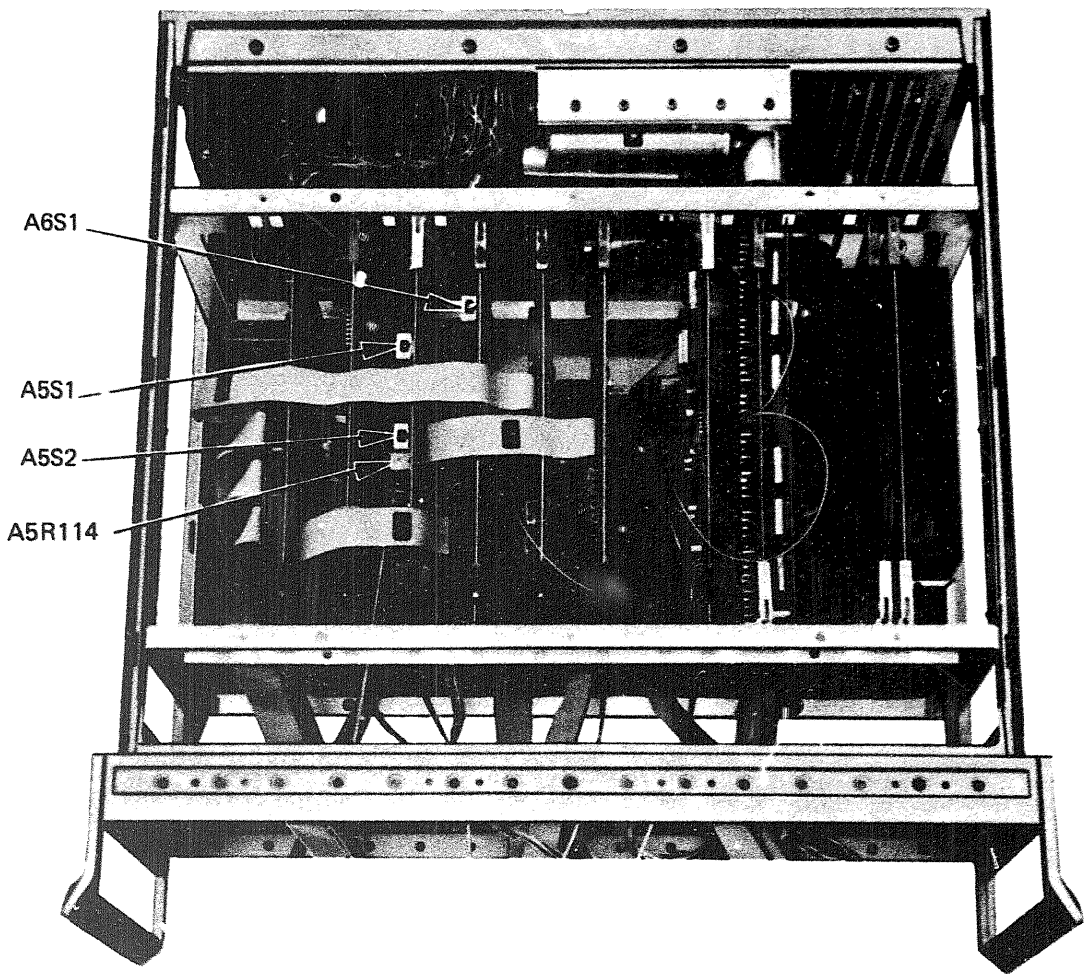


Figure 3–12. Location of internal controls.